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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

KEBEDE, BROOK

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 01/28/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/123,430

Applicant(s)

YATES, DONALD L. *shc*

Examiner

Brook Kebede

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 December 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,6,7,9-15,17,18,20-27,44,52,58 and 61-77 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13,23,52,58,65,66,72 and 73 is/are allowed.
- 6) ☒ Claim(s) 1,6,7,9-12,14,15,17,18,20-22,24-27,44,61-64,67-71 and 74-77 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 13, 2002 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 6, 7, 9, 14, 17, 18, 20, 24, 26, 44, 61, 68, 75, 76 and 77 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishizawa et al., (USPAT/5,275,184).

Re claim 1, Nishizawa et al. disclose a method for removing surface contaminants from air/liquid interface of a semiconductor processing bath (i.e., an etching bath) for processing semiconductor wafers the method comprising immersing wafers in a bath of semiconductor processing fluid; and reducing volume of semiconductor processing fluid in the bath by rapidly displacing an upper portion semiconductor processing fluid present in the bath while the wafers are immersed in the bath (see Fig. 2 and Col. 2, lines 62-67 through Col. 5, lines 1-27 and see abstract).

Re claim 6, as applied to claim 1 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the contaminants include silica (see Fig. 2).

Re claim 7, Nishizawa et al. disclose a method for reducing the contamination on a semiconductor wafer from wet etching bath comprising: processing the semiconductor wafer in the wet etching bath containing and etching fluid; subsequently rapidly reducing a volume of said wet etching bath by removing a substantial portion of an upper portion of the etching fluid from the wet etching bath to remove surface contaminants from an air/liquid interface of the wet etching bath while retaining the semiconductor wafer in the etching bath and subsequently removing of the wafer from the bath (see Fig. 2 and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14).

Re claim 9, as applied to claim 7 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the upper portion of the etching fluid is removed by draining a top portion of the etching fluid from wet etching bath (see Fig. 2 and related text in Col. 7, lines 2-14).

Re claim 14, Nishizawa et al. disclose a method for removing contaminants from an air/liquid interface of a semiconductor processing bath (i.e., an etching bath) for processing semiconductor wafers the method comprising: rapidly removing an upper portion of a semiconductor processing fluid present in the bath while the wafers are in the bath by rapidly removing a wafer boat containing the semiconductor wafer from the bath to remove the surface contaminants from air/liquid interface (see Fig. 2).

Re claim 17, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing an aqueous hydrofluoric acid etching fluid into a wet etching vessel; immersing the semiconductor fluid into wet etching fluid; contacting the semiconductor wafer with the etching fluid for period or time; reducing a volume of the etching fluid in which the wafers are immersed by rapidly removing a portion of the

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etching fluid from the upper surface of wet etching vessel while keeping the semiconductor wafer immersed in the etching fluid (see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14; Col. 11, lines 18-20).

Re claim 18 as applied to claim 17 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the semiconductor is a silicon wafer (see abstract)

Re claim 20, as applied to claim 17 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the etching fluid is removed from an upper surface of the wet etching vessel by draining of the top portion of the etching fluid from the wet etching vessel (see Fig. 2 and related text in Col. 7, lines 2-14).

Re claim 24, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing and etching fluid into a wet etching vessel; placing the semiconductor fluid into wet etching fluid; contacting the semiconductor wafer with the etching fluid for period or time; rapidly removing a portion of the etching fluid from the upper surface of wet etching vessel by rapidly removing a wafer boat containing the semiconductor wafers from the wet etching vessel (see Fig. 2).

Re claim 26, as applied to claim 17 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the etching fluid is removed from the upper surface of the wet etching vessel by physically removing a top portion of the etching fluid from the wet etching bath (see Fig. 2).

Re claim 44, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: immersing a wafer boat suspended on a lifting arm in an etching vessel having an etching fluid (i.e., an aqueous HF) therein for sufficient time to

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etch the silicon wafer; and rapidly removing the wafer boat from the etching vessel to remove the contaminants residing on the upper surface of the aqueous HF solution by an upward movement of the arm and causing the etching fluid to spill out of the vessel fluid (see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14; Col. 11, lines 18-20).

Re claim 61, Nishizawa et al. disclose a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers, said method comprising: reducing a volume of the semiconductor processing bath by rapidly removing an upper portion of a semiconductor processing fluid present in said bath, while said wafers are in said bath, to permit flow of said upper portion of said processing fluid and thereby break eddy currents holding said surface contaminants at said air/liquid interface (see Fig. 2).

Re claim 68, Nishizawa et al. disclose a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers, said method comprising: reducing a volume of the semiconductor processing bath by rapidly removing an upper portion of a semiconductor processing fluid present in said bath, to permit flow of said upper portion of said processing fluid and thereby while said wafers are in said bath, to break surface tension forces holding said surface contaminants at said air/liquid interface (see Fig. 2).

Re claim 75, Nishizawa et al. disclose a method for reducing the contamination on a semiconductor wafer from a wet etching bath comprising: processing said semiconductor wafer in said wet etching bath containing an etching fluid; subsequently reducing a volume of etching fluid in the wet etching bath and breaking eddy currents of

said wet etching bath by rapidly removing an upper portion of said etching fluid from said wet etching bath, said act of breaking said eddy currents further releasing surface contaminants which are formed at an air/liquid interface of said wet etching bath and held at said air/liquid interface by said eddy currents; and subsequently removing said semiconductor wafer from said wet etching bath (see Fig. 2).

Re claim 76, Nishizawa et al. disclose a method for reducing the contamination on a semiconductor wafer from a wet etching bath comprising processing said semiconductor wafer in said wet etching bath containing an etching fluid; subsequently reducing a volume of etching fluid in the wet etching bath and breaking surface tension forces of said wet etching bath by rapidly removing an upper portion of said etching fluid from said wet etching bath, said act of breaking said surface tension forces further releasing surface contaminants which are formed at an air/liquid interface of said wet etching bath and held at said air/liquid interface by said eddy currents; and subsequently removing said semiconductor wafer from said wet etching bath (see Fig. 2).

Re claim 77, Nishizawa et al. disclose a method for reducing the contamination on a semiconductor wafer, said method comprising: processing said semiconductor wafer in a static etching bath containing an etching fluid; and reducing a volume of the etching fluid by rapidly removing an upper portion of said etching fluid while said semiconductor wafer is in said static etching bath (see Fig. 2).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

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the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 10, 27, 62, and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al., USPAT/5,275,184 in view of Itoh et al., USPAT/5,795,401.

Re claim 10, Nishizawa et al. teach all the limitation in the claimed limitations, as applied in claim 7, except the use of paddle to remove the fluid from the top portion of the etching process bath.

Itoh et al. disclose the use of back paddle to jet (remove) out the wash fluid during process of cleaning of semiconductor substrate (see related text in Col. 10, lines 18-48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with paddle as taught by Itoh et al. because the use of paddle would have provided removing of contaminants from the top of the wafer etching bath.

Re claim 27, Nishizawa et al. teach all the limitation in the claimed invention, as applied in claim 26, except the use of paddle to remove the fluid from the top portion of the etching process bath.

Itoh et al. disclose the use of back paddle to jet (remove) out the wash fluid during process of cleaning of semiconductor substrate (see related text in Col. 10, lines 18-48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with paddle as taught by Itoh et al. because the use of paddle would have provided removing of contaminants from the top of the wafer etching bath.

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Re claim 62, as applied to claim 61 above, Nishizawa et al. teach all the limitation in the claimed limitations except the use of paddle to remove the fluid from the top portion of the etching process bath.

Itoh et al. disclose the use of back paddle to jet (remove) out the wash fluid during process of cleaning of semiconductor substrate (see related text in Col. 10, lines 18-48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with paddle as taught by Itoh et al. because the use of paddle would have provided removing of contaminants from the top of the wafer etching bath.

Re claim 69, as applied to claim 68 above, Nishizawa et al. teach all the limitation in the claimed limitations except the use of paddle to remove the fluid from the top portion of the etching process bath.

Itoh et al. disclose the use of back paddle to jet (remove) out the wash fluid during process of cleaning of semiconductor substrate (see related text in Col. 10, lines 18-48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with paddle as taught by Itoh et al. because the use of paddle would have provided removing of contaminants from the top of the wafer etching bath.

6. Claims 11, 21, 63 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al., USPAT/5,275,184 in view of Mohindra et al., USPAT/5,958,146.

Re claim 11, Nishizawa et al. disclose a method for removing contaminants from a semiconductor processing bath (i.e., an etching bath) for processing semiconductor

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wafers the method comprising: rapidly reducing a volume of the wet etching bath by rapidly removing an upper portion of a semiconductor processing fluid presented in the bath, while the wafer in the bath (see Fig. 2). However, Nishizawa et al. do not mention use of valve to remove the etching fluid.

Mohindra et al. disclose the use of valve to remove during cleaning (etching) process of the semiconductor wafer (see related text in Col. 3, lines 56-60).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a valve as taught by Mohindra et al. because the use of valve would have provided another method of removing contaminants from the top of the wafer etching bath when the valve opens by mechanical means.

Re claim 21, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing an etching fluid into a wet etching vessel; placing the semiconductor wafer in the etching fluid; contacting the semiconductor wafer with the etching fluid for a period of time; and reducing a volume of the etching fluid by rapidly removing a portion of the etching fluid from the upper surface of the wet etching vessel (see Fig. 2). Nishizawa et al. do not specifically mention use of valve to remove the etching fluid.

Mohindra et al. disclose the use of valve to remove during cleaning (etching) process of the semiconductor wafer (see related text in Col. 3, lines 56-60).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a valve as taught by Mohindra et al. because the use of valve would have provided

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removing of contaminants from the top of the wafer etching bath when the valve opens by mechanical means.

Re claim 63, as applied to claim 61 above, Nishizawa et al. disclose all the claimed limitations except the use of valve.

Mohindra et al. disclose the use of valve to remove during cleaning (etching) process of the semiconductor wafer (see related text in Col. 3, lines 56-60).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a valve as taught by Mohindra et al. because the use of valve would have provided removing of contaminants from the top of the wafer etching bath when the valve opens by mechanical means.

Re claim 70, as applied to claim 68 above, Nishizawa et al. disclose all the claimed limitations except the use of valve.

Mohindra et al. disclose the use of valve to remove during cleaning (etching) process of the semiconductor wafer (see related text in Col. 3, lines 56-60).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a valve as taught by Mohindra et al. because the use of valve would have provided removing of contaminants from the top of the wafer etching bath when the valve opens by mechanical means.

7. Claims 12, 15, 22, 25, 64, 67, 71 and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al. (USPAT/5,275,184) in view of Hayami et al. (USPAT/5,474,616).

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Re claim 12, Nishizawa et al. disclose a method of removing contaminants from a semiconductor processing cleaning bath for processing semiconductor wafers the method comprising: reducing a volume of fluid in the semiconductor processing cleaning bath by rapidly removing an upper portion of a semiconductor processing fluid present in the bath, while the wafers are in the bath (see Fig. 2). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching bath when the door opened.

Re claim 15, Nishizawa et al. disclose a method of removing contaminants from a semiconductor processing cleaning bath for processing semiconductor wafers the method comprising: rapidly removing an upper portion of a semiconductor processing fluid present in the bath, while the wafers are in the bath (see Fig. 2). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.
(see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of telescopically collapsing sidewalls would have provided removing of contaminants from the top of the wafer etching bath when the sidewall folded.

Re claim 22, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing and etching fluid into a wet etching vessel; placing the semiconductor fluid into wet etching fluid; contacting the semiconductor wafer with the etching fluid for period or time; rapidly removing a portion of the etching fluid from the upper surface of wet etching vessel while keeping the semiconductor wafer immersed in the etching fluid (see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference

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with a hingedly released door as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching bath when the door opened.

Re claim 25, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing an etching fluid (i.e., an aqueous HF solution) into a wet etching vessel; placing the semiconductor fluid into wet etching fluid; contacting the semiconductor wafer with the etching fluid for period or time; and reducing a fluid-containing volume of the wet etching vessel so as to rapidly displace a portion of the etching fluid from the upper surface of wet etching vessel at a non-constant velocity while keeping the semiconductor wafer immersed in the etching fluid (see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14).

However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

(see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of telescopically collapsing sidewalls would have provided removing of contaminants from the top of the wafer etching bath when the sidewall folded.

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Re claim 64, as applied to claim 61 above, Nishizawa et al. disclose all the claimed limitation. However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching bath when the door opened.

Re claim 67, as applied to claim 61 above, Nishizawa et al. disclose all the claimed limitations. However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

(see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of telescopically

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collapsing sidewalls would have provided removing of contaminants from the top of the wafer etching bath when the sidewall folded.

Re claim 71, as applied to claim 68 above, Nishizawa et al. disclose all the claimed limitation. However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching bath when the door opened.

Re claim 74, as applied to claim 68 above, Nishizawa et al. disclose all the claimed limitations. However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

(see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of telescopically collapsing sidewalls would have provided removing of contaminants from the top of the wafer etching bath when the sidewall folded.

Allowable Subject Matter

8. Claims 13, 23, 52, 58, 65, 66, 72 and 73 are allowed over prior art of record.

Response to Arguments

9. Applicants' arguments filed on December 13, 2002 have been fully considered but they are not persuasive.

Applicants' arguments are redundant and similar to the previous arguments and for that reason the Examiner respectfully would like to incorporate herein the Examiner's response to applicants argument that was mailed in the Office actions of Paper No. 10, 20 and 27 by reference. Further, in response to applicants' argument that "Nishizawa et al. does not teach or suggest removing a surface contaminant by *reducing a volume of said semiconductor processing bath ...*," the Examiner respectfully submits that Nishizawa et al. disclose reducing the volume of cleaning solution. Although Nishizawa et al. process provides continuous supply of cleaning fluid, the volume of the cleaning (etching) fluid is reduced when the wafer immersed and that is inherent process within Nishizawa et al. disclosure. Therefore, the alleged process is within the scope of Nishizawa et al. disclosure.

Conclusion

10. **THIS ACTION IS MADE NON-FINAL.**

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Correspondence

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede

BK
January 26, 2003

Olik Chaudhuri
Olik Chaudhuri
Supervisory Patent Examiner
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